What is claimed is:

1. A method of fabricating an X-ray detector array, comprising:

providing a substrate having a capacitor area and a transistor area;

forming a gate line extending transversely on the substrate, wherein the gate line includes a gate electrode in the transistor area;

forming a gate insulation layer on the gate line, the gate electrode, and the substrate;

forming a semiconducting island on the gate insulation layer in the transistor area;

forming a common line and a data line extending longitudinally on the gate insulation layer, and forming a source electrode and a drain electrode on the semiconducting island to form a thin film transistor (TFT) structure, wherein the drain electrode electrically connects the data line;

forming a planarization layer on the gate insulation layer, the common line, the TFT structure, the data line, and the gate line;

forming a first conductive layer on the planarization layer in the capacitor area;

forming a dielectric layer on the first conductive layer and the planarization layer;

forming a first via hole and a second via hole penetrating the dielectric layer and the planarization layer, wherein the first via hole exposes a surface of the source electrode, and the second via hole exposes part of a surface of the first conductive layer and part of a surface of the common line; and

forming a conformal second conductive layer on the dielectric layer, an interior surrounding surface of the first via hole and an interior surrounding surface of a second via hole.

2. The method according to claim l, wherein the gate line is metal.

3. The method according to claim 1, wherein the gate insulation layer comprises one of SiO_2, SiN_x, and SiON.

4. The method according to claim 1, wherein the forming of the semiconducting island comprises:

forming an amorphous silicon layer on the gate insulation layer;

forming a doped amorphous silicon layer on the amorphous silicon layer; and

removing part of the doped amorphous silicon layer and the amorphous silicon layer to form the semiconducting island in the transistor area.

5. The method according to claim 4, further comprising, after forming the common line, the data line, and the TFT structure:

using the source electrode and drain electrode as a mask, and removing part of the doped amorphous silicon layer to expose a surface of the amorphous silicon layer.

6. The method according to claim 1, wherein the common line, the data line, the source electrode, and the drain electrode are simultaneously defined by photolithography.

7. The method according to claim l, wherein the planarization layer is one of a spin-on-glass (SOG) and organic layer.

8. The method according to claim 1, wherein the first conductive layer comprises one of indium tin oxide (ITO) and indium zinc oxide (IZO), serving as one of a bottom electrode and a pixel electrode.

9. The method according to claim 1, wherein the dielectric layer comprises one of SiO_2, SiN_X, and SiON.

10. The method according to claim 1, wherein the second conductive layer comprises one of indium tin oxide (ITO) and indium zinc oxide (IZO), serving as one of a top electrode and a charge collector electrode.

11. The method according to claim 1, wherein the gate line has a protruding portion in the transistor area, serving as the gate electrode.

12. The method according to claim 1, wherein the gate line located in the transistor area serves as the gate electrode.

13. The method according to claim 1, further comprising, in the forming of the first conductive layer:

simultaneously forming a second opening in the first conductive layer, wherein the second opening exposes the planarization layer above the common line.

14. The method according to claim 13, wherein the second via hole and the second opening overlap.

15. A method of fabricating an X-ray detector array, comprising:

providing a substrate having a capacitor area and a transistor area;

forming a gate line extending transversely on the substrate, wherein the gate line includes a gate electrode in the transistor area;

forming a gate insulation layer on the gate line, the gate electrode, and the substrate;

forming a semiconducting island on the gate insulation layer in the transistor area;

forming a common line and a data line extending longitudinally on the gate insulation layer, and forming a source electrode and a drain electrode on the

semiconducting island to form a thin film transistor (TFT) structure, wherein the drain electrode electrically connects the data line;

forming a planarization layer on the gate insulation layer, the common line, the TFT structure, the data line, and the gate line;

forming a first conductive layer on the planarization layer in the capacitor area, wherein the first conductive layer has a first opening to expose the planarization layer above the common line;

forming a dielectric layer on the first conductive layer and the planarization layer;

forming a first via hole and a second via hole penetrating the dielectric layer and the planarization layer, wherein the first via hole exposes a surface of the source electrode, the second via hole exposes part of a surface of the first conductive layer and part of a surface of the common line, and the second via hole and the first opening have an overlap;

forming a conformal second conductive layer on the dielectric layer, an interior surrounding surface of the first via hole and an interior surrounding surface of the second via hole; and

removing part of the second conductive layer to form a third conductive layer, a fourth conductive layer, and a second opening, wherein the third conductive layer is isolated from the fourth conductive layer by the second opening;

16. The method according to claim 15, wherein the forming of the semiconducting island comprises:

forming an amorphous silicon layer on the gate insulation layer;

forming a doped amorphous silicon layer on the amorphous silicon layer; and removing part of the doped amorphous silicon layer and the amorphous silicon layer to form the semiconducting island in the transistor area.

17. The method according to claim 16, further comprising, after the forming of the common line, the data line, and the TFT structure:

using the source electrode and drain electrode as a mask, and removing part of the doped amorphous silicon layer to expose a surface of the amorphous silicon layer.

18. The method according to claim 15, wherein the gate line has a protruding portion in the transistor area, serving as the gate electrode.

19. The method according to claim 15, wherein the gate line located in the transistor area serves as the gate electrode.

20. A method of fabricating an X-ray detector array, used to decrease consumption of masks during photolithography, comprising:

providing a substrate having a capacitor area and a transistor area;

using a first mask to form a gate line transversely extending on the substrate by photolithography, wherein the gate line includes a gate electrode in the transistor area;

forming a gate insulation layer on the gate line, the gate electrode and the substrate;

using a second mask to form a semiconducting island on the gate insulation layer in the transistor area by photolithography;

using a third mask to form a common line and a data line longitudinally extending on the gate insulation layer by photolithography, and forming a source electrode and a drain electrode on the semiconducting island to form a thin film

transistor (TFT) structure, wherein the drain electrode electrically connects the data line;

forming a planarization layer on the gate insulation layer, the common line, the TFT structure, the data line and the gate line;

using a fourth mask to form a first conductive layer on the planarization layer in the capacitor area by photolithography;

forming a dielectric layer on the first conductive layer and the planarization layer;

using a fifth mask to form a first via hole and a second via hole penetrating the dielectric layer and the planarization layer by photolithography, wherein the first via hole exposes a surface of the source electrode, the second via hole exposes part of a surface of the first conductive layer and part of a surface of the common line;

forming a conformal second conductive layer on the dielectric layer, an interior surrounding surface of the first via hole and an interior surrounding surface of the second via hole; and

using a sixth mask to remove part of the second conductive layer to form a third conductive layer, a fourth conductive layer and a first opening by photolithography, wherein the third conductive layer is isolated from the fourth conductive layer by the first opening;

wherein the first conductive layer electrically connects the common line by the fourth conductive layer.